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Low Power FinFET Based Full Adder Design

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Abstract: The great challenge in the nanometer regime is due to Short Channel Effects that cause an exponential increase in the leakage current. With the advancement in technology, Conventional CMOS has Short Channel Effects. In order to reduce the Short Channel Effects, FinFET is used. FinFETs are the new emerging transistors that can work in the nanometer range to overcome these Short Channel Effects. The Low Power FinFET based Full Adder is implemented by using CADENCE VIRTUOSO tools in 45nm technology with the supply voltage of 1V in CMOS and 15nm technology with the supply voltage of 0.7V in FinFET. The Simulation is done to compare power, delay and power- delay product. The result shows that the PDP of GDI FinFET Full Adder is reduced to 67% compared to FinFET Full Adder.

Keywords: Low Power; Full Adder; CMOS; FinFET; GDI.

I. INTRODUCTION

The batteries driven and portable devices are of a great demand in many industrial applications which need the implementation of low power and area efficient devices [1, 2]. Moore's law was discovered by Gordon Moore in 1965. He was the Co-founder of INTEL Corporation. He has set the pace for our modern digital revolution and utilized that the computing world increases in power and decreases in cost. He has predicted that number of transistors in an integrated circuit would quadruple for every two years. This prediction is known as Moore's Law. Today, many of the industrial applications are designed in nanometer range. The transistor size is restricted with the phenomena like Short Channel Effects which include hot carrier effect and tunneling through oxide thickness.
In CPU, arithmetic logic unit (ALU) is a crucial part. The adder cell is an important unit of an ALU. Many digital circuit adders are used to perform addition of numbers [3, 8]. In many computers, adders are used in other parts of the processor to calculate addresses [6], table indices and similar operations. Due to the increase in the demand of portable devices such as mobile phones, lap top, tablets [9, 10], and the need of area and power efficient VLSI circuits is arisen. Low power adder cells are used in Low power applications. In this paper, an improved 1-bit full adder circuit is implemented which consumes reduced power and very less number of transistors.

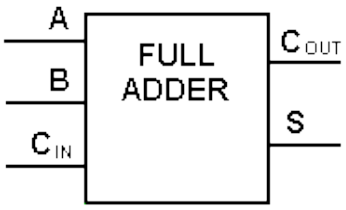

Fig.1. Single bit Full Adder

A 1-bit Full adder circuit consists of three inputs A, B, and Cin. The third input Cin is called carry input. The Full adder is usually a component in cascade of adders which adds binary numbers. The Block diagram representation of full adder is shown in the Fig.1. It consists of two outputs sum and carry output.

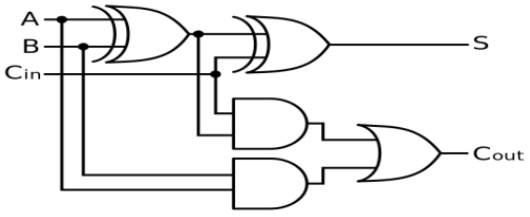

Fig.2. Logic Diagram of 1-bit CMOS Full Adder

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The Logic Diagram of 1-bit CMOS Full Adder can be constructed by using two EX-OR gates, two AND gates, and one OR gate. The expressions for SUM and Carry output are

SUM=A xor B xor Cin
Carry=A and B + Cin(A xor B)

Table 1: Truth Table for 1-bit Full Adder

A	B	Cin	SUM	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The Truth Table for 1-bit Full adder is shown in the Table 1.With the help of this truth table we can easily implement Full Adder Logic.

II. FINFET

FinFET means Fin Field Effect Transistor. FinFET is a Non Planar Dual Gate Transistor used in the Silicon Architecture which consists of very large computational density. FinFET was coined by Berkeley researchers of university of California and it was developed for the use of Silicon-on-Insulator.

FinFET technology takes its name from the fact that the FET structure used looks like a set of fins when viewed. The main characteristic of the FinFET is that it has a conducting channel wrapped by a thin silicon "fin" from which it gains its name [3]. The thickness of the fin determines the effective channel length of the device.

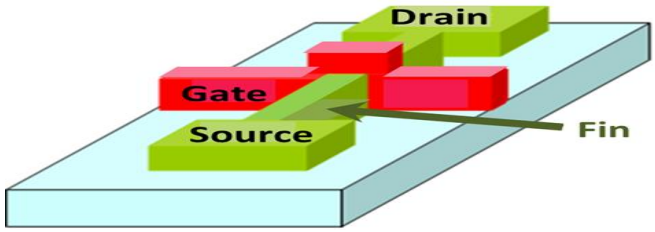

Fig. 3: FinFET Structure

The attractiveness of FinFET is 3D structure that rises above the planar substrate giving more volume than a planar gate for same planar area. FinFET is used to conduct channel that rise above the insulator, thin silicon structure, shaped like Fin called gate electrode. This gate electrode operates on a single transistor. In contrast to a Planar the source and Drain channel is built by three dimensions on the top of the silicon substrate called as Fin. MOSFET FinField Effect techniques are promising substitutes for bulk CMOS at nanoscale.

A. Single Bit FinFET Full Adder

The FinFET based full adder in various cells can be investigated in terms of performance and energy efficiency. 1-bit FinFET Full adder can be designed for four reasons such as power dissipated, delays, power delay product, and energy delay product.

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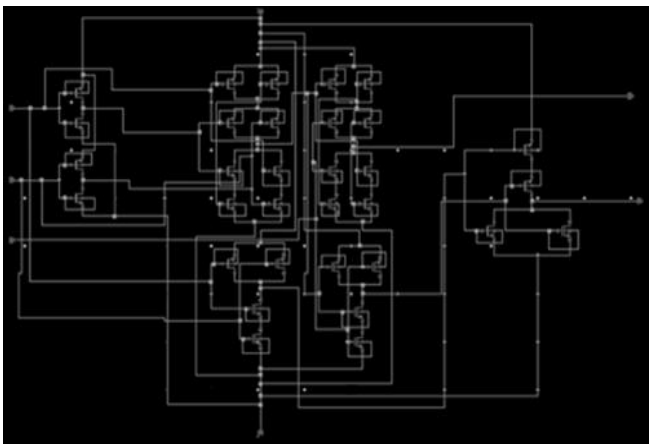

Fig. 4: Single Bit FinFET Full Adder

Single bit FinFET full adder using transistor level diagram is shown in Fig. 4. The main reason for FinFET is to decrease the leakage power. Using two EX-OR gates, two AND gates and one OR gate FinFET single bit Full ADDER is implemented.
The main advantage of FinFET full adder is Low cost, suppressed Short channel effects and Better in Driving current.
In digital circuits, Full adders are used extensively. The performance of 1-bit full adder is benchmarked against conventional CMOS full adder. The FinFET based full adder shows a large reduction in delay and provided the device with high speed performance which is better than the conventional CMOS Full Adder. The FinFET has better and faster switching speed due to the presence of multiple gates in the FinFET structure and drives more current compared to MOSFET structure. The main advantage of FinFET full adder is Low cost, suppressed Short channel effects and Better in Driving current.

III. IMPLEMENTATION OF GDI USING FULL ADDER

B. GDI Operation

GDI is nothing but Gate Diffusion Input Technique. This type of technique is suitable for lower delay and designing a circuit with reduced power. This is because the technique helps to decrease the transistor count when compared with CMOS and other obtainable low power methods.

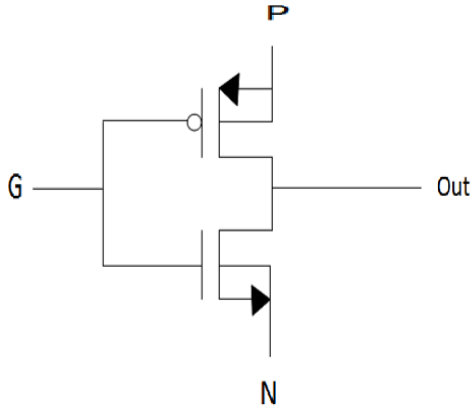

Fig. 5: Basic GDI Cell

GDI cell contains three input operations they are
G (Common gate input of Nmos and Pmos)
P (Input to the source/drain of Pmos)
N (Input to the source/drain of Nmos)
Bulks of NMOS and PMOS are connected to vss and vdd respectively [4,5,6].

C. Functions of GDI Cell

The GDI cell with four ports will be recognized as replacement multi-functional device, which may attain six functions with simply totally different combinations of input G, P and N.

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It must be remarked that not all the functions are possible in standard p-well CMOS process, but can be successfully implemented in twin well CMOS or Silicon-on-Insulator technologies.

Table 2: Functions of GDI cell

N	P	G	OUTPUT	FUNCTION
0	1	A	A’	INVERTER
0	B	A	A’B	F1
B	1	A	A’+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	A’B+A’C	MUX
B’	B	A	A’B+B’A	XOR
B	B’	A	AB+A’B’	XNOR

Table 2 shows different functions of Gate Diffusion Input Technique with different combinations G, P and N [7]. With the help of these special functions, table logic gates can be implemented with few transistors mostly in GDI when compared with Complementary Metal oxide Semiconductor process.

EX-OR gate using GDI cell

The EX-OR circuit created with the assistance of GDI cell is an application of the GDI technique. For example EX-OR gate which has 8 transistors compared to conventional CMOS. As shown in the Fig. 6, the EXOR created exploitation GDI technique needs solely four transistors (2PMOS & 2NMOS). GDI EX-OR circuit uses less transistors compared with the traditional CMOS EX-OR Gate.

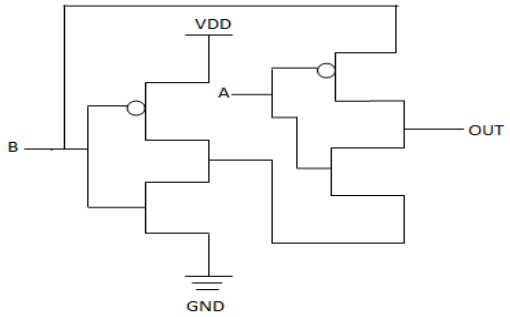

Fig. 6: GDI using EX-OR Gate

IV. GDI USING CMOS AND FINFET FULL ADDER

GDI CMOS Full Adder

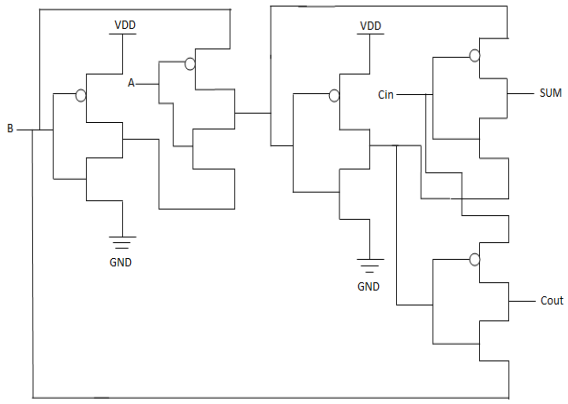

Fig. 7: GDI CMOS Full Adder

GDI full adder contains three input pins A, B and Cin and two output pins sum and Cout. It is built from two XOR gates and one MUX. GDI full adder is implemented based on some special functions given in the table. In GDI full

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adder, power dissipation plays an important role in high performance applications. The full adder cell using transistors is already explained. GDI has suffered from practical limitations like swing degradation. In the first stage of this cell, the GDI technique is used for generating of XOR and XNOR functions. The full adder cell using transistors is already explained. The GDI technique needs solely 8 transistors 4PMOS and 4NMOS.
GDI Full adder generates expressions for SUM and CARRY [7]. It was used based on the special functions table. While using the Logic Function MUX as selective input, the carry logic is implemented.
When input N=C, P=B, G=A these are the inputs seen in the functions table. Instead of this replacing N=B, P=Cin, G= A XNOR B.
Output=A'B+AC Mux function. So substituting the values we get carry function
(A XOR B) Cin + (A XNOR B) B
(AB' + A'B) Cin + B (AB + A'B')
(A XOR B) Cin + AB (This is the carry expression)
SUM=A XOR B XOR Cin
CARRY= (A XOR B) Cin + AB
Using the two expressions FinFET Full Adder is implemented by using Gate Diffusion Input Technique.

GDI FinFET Full Adder

The Gate Diffusion Input Technique decreases both delay and power.GDI FinFET full adder consists of three input pins and two output pins. Here we are using shorted gate FinFET according to the modes of operation. The supply voltage is taken as 0.7V for GDI FinFET using cadence Virtuoso tool at 15nm technology. In GDI FinFET multiplexer is taken as selective input. Multiplexer looks like an inverter in order to generate the carry expression we definitely use multiplexer. FinFET GDI doesn't achieve full swing because of the threshold voltage loss. Another reason for GDI FinFET is we are taking three inputs without the use of VDD and GND. The Gate Diffusion Input Technique would possibly enrich the tool chest of VLSI Designers.

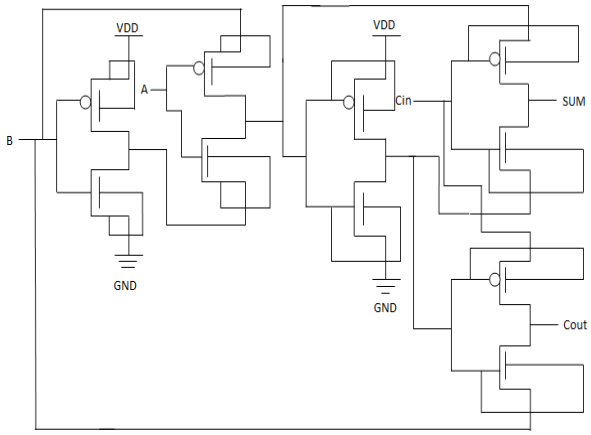

Fig. 8: GDI FinFET Full Adder

V. SIMULATION RESULTS

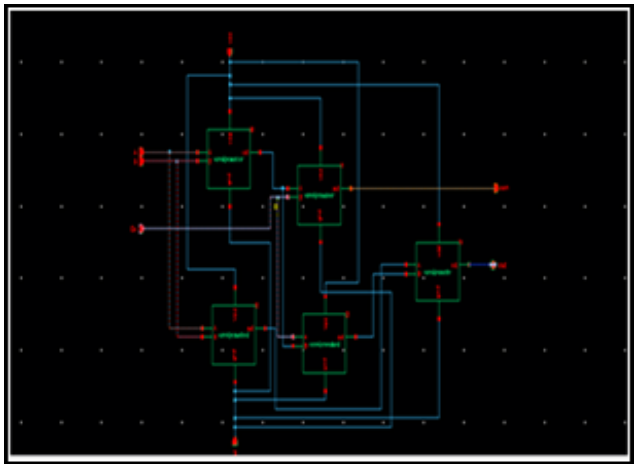

Fig. 9: Schematic Diagram for CMOS Full Adder

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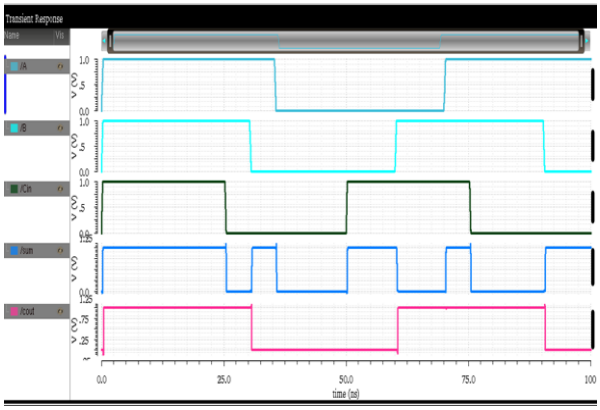

Fig. 10: Output Wave Form for CMOS Full Adder

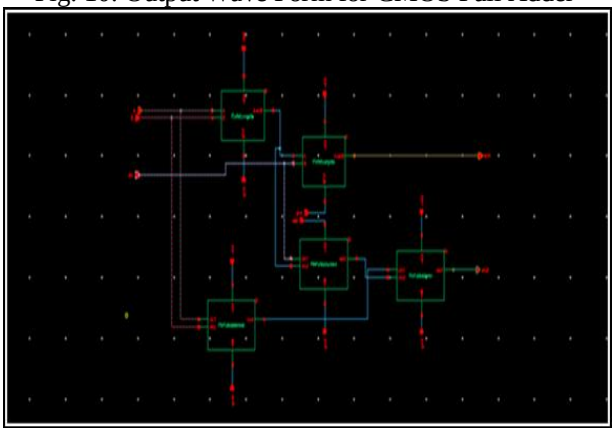

Fig. 11: Schematic Diagram for FinFET Full Adder

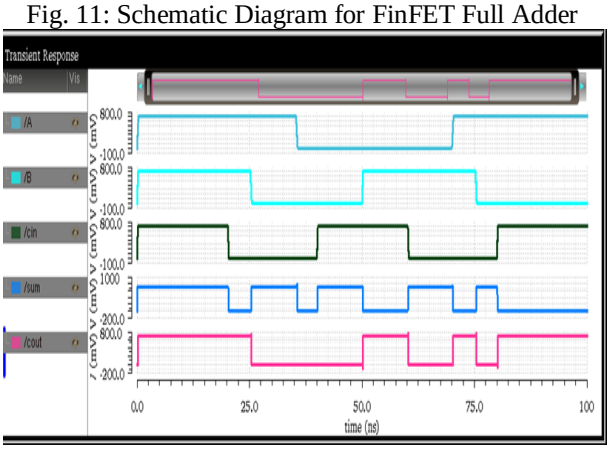

Fig. 12: Output Wave Form for FinFET Full Adder

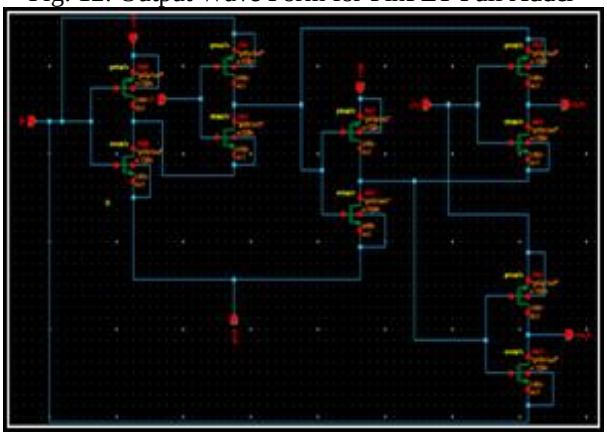

Fig. 13: Schematic Diagram for GDI CMOS Full Adder

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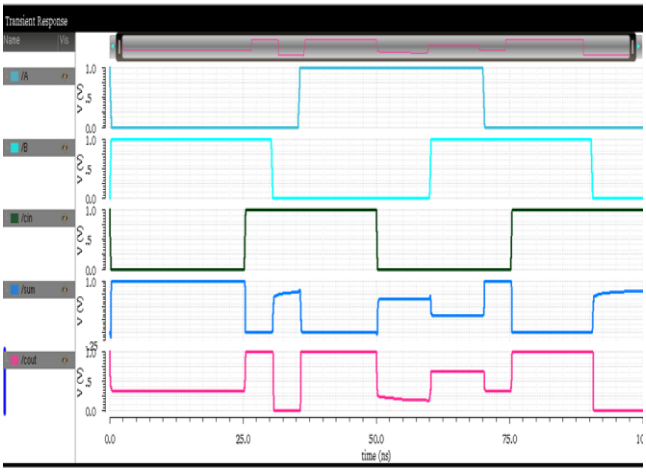

Fig. 14: Output Waveform for GDI CMOS Full Adder

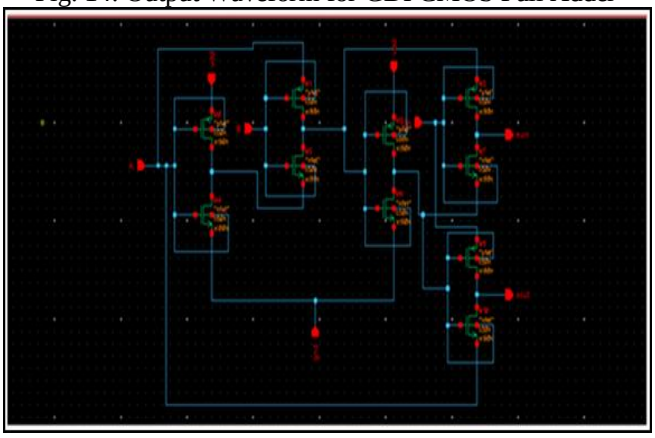

Fig. 15: Schematic Diagram for GDI FinFET Full Adder

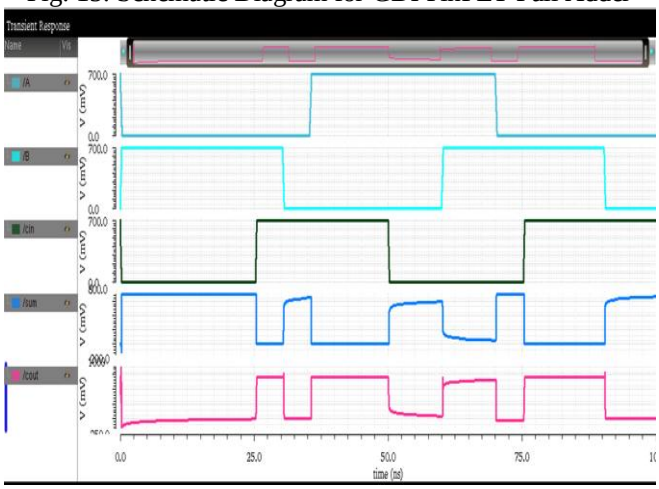

Fig. 16: Output Waveform for GDI FinFET Full Adder

VI. COMPARISON VALUES [45NM TECHNOLOGY]

Table 4: Comparison Values for CMOS & GDI Full Adder [45nm Technology]

	CMOS Full Adder	GDI CMOS Full Adder
Delay(ps)	69.12	108.7
Power(nW)	399.2	107.4
Power-Delay Product	27592.7×10^{-21}	11674.3×10^{-21}
No. of Transistor Count	32	10

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VII. COMPARISON VALUES [15NM TECHNOLOGY]

Table 3: Comparison Values for FinFET and GDI Finfet Full Adder [15nm Technology]

	FinFET Full Adder	GDI FinFET Full Adder
Delay(ps)	84.32	80.92
Power(nW)	40.9	13.81
Power-Delay Product	3448.68×10^{-21}	1117.50×10^{-21}
No. of Transistor Count	32	10

VIII. CONCLUSION

In this Project, Different Full Adder circuits are implemented by using CMOS, FinFET, GDI CMOS and GDI FinFET and Simulated in CADENCE VIRTUOSO TOOLS using 45nm Technology with the supply voltage of 1V for CMOS and GDI CMOS Full Adder and 15nm Technology with the supply voltage of 0.7 V for FinFET and GDI FinFET Full adder.

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